Examination of digital circuits with simulation and measurement

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Abstract: We teach Digital Technology to the Students of the Óbuda University AMK for many years. In the curriculum there are lectures and laboratory exercises. Initially, all the measurements were performed with an oscilloscope, but later part of the measurements were simulated. From here came the idea to examine the operation of the logic circuits by simulation, then oscilloscope, and compare the results. We also made comparisons for combination and sequential networks. The results of this work are described in the article.

I. TESTED CIRCUITS

A. Combination circuits

The equation for the output of the first tested combination network: $Y = \overline{C * B + B * \overline{A}}$

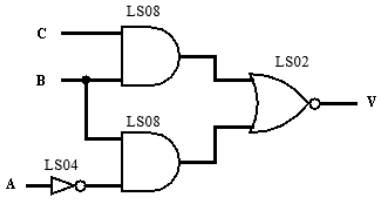


Figure 1 Simple combination circuit

We connected tri state outputs, in the second tested combination network. Such outputs should only be connected if it is necessary to ensure that only one gate is enabled at a time. This is achieved by the B and C inputs of the corresponding control.
If the upper gate is enabled, the input A is displayed on the output, if the lower gate is enabled, the input A negated is displayed on the output.

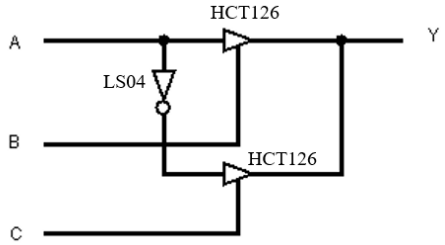


Figure 2 Tri state output

The third examined combination network is a full adder.
The equation of the output:
$Si = A * B + (A + B) * Ci$
$Ci = A \oplus B \oplus Ci$

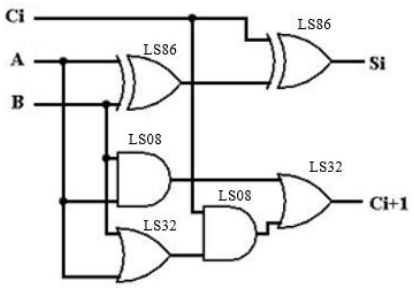
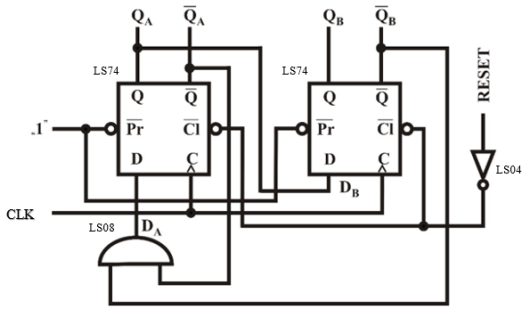


Figure 3 Full adder

B. Sequential circuits

The first sequential circuit is a network of two D flip flops. Reset the network to 0, then from there to the rising edge of clock 1, 2 and again 0.



Figurer 4 Sequential circuit with flip flop

The second sequential circuit contains a shift register, its name is ring counter. Reset is loaded on the 1, then on the rising edge of the clock, the 2, 4, 8, and again 1 states the network.

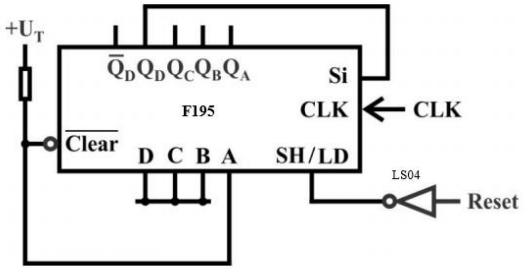


Figure 5 Ring counter

The third sequential circuit contains a decimal synchronous counter. Reset is deleted, that is synchronous, that is, the rising edge of the clock. Reset 0, 1, 2, 3, 4, 5, and 0 again.

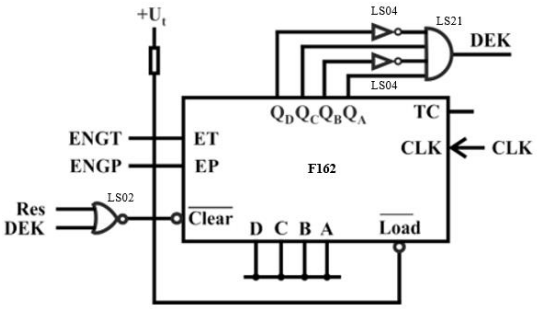


Figure 6 Sequential circuit with synchronous counter

II. THE PROGRAMS USED FOR THE SIMULATION

A. Logisim

Logisim is an open source program. It is free download and you do not have to install it immediately to run. We were looking for a program which can be used easily, by which we can demonstrate the function of the digital electronic circuits. So we found the Logisim program. It is easy to operate and has a transparent design. It was for educational purposes. The simple toolbar interface and the simulation of circuits make it easy to get familiar with the most important concepts related to logical circuits. It runs on any machine that supports Java 5 or later. Color coded leads help to simulate and troubleshoot a circuit. The finished circuits can be saved in a file, exported to a GIF file, or printed. We tested the operation of our circuits with this program.

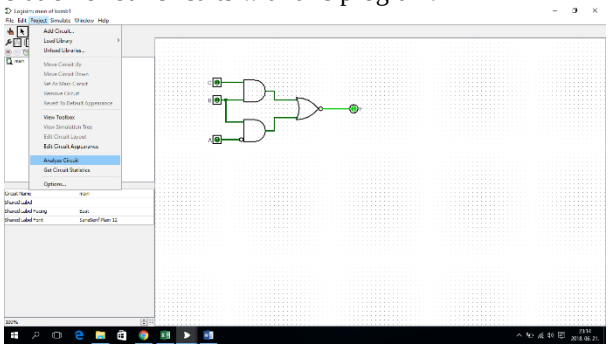


Figure 7 Logisim program

B. ISIM simulator

The Xilinx ISE WebPack (Integrated Software Environment) is a free software developed by Xilinx for FPGAs and CPLDs, which is freely downloadable from the internet at the company's website. The development system includes all the elements needed for circuit diagram basis and hardware description language basis to development. The designer his ideas, his plans:

- can input it in Schematic, using the wiring diagram creation and input program.
- can enter hardware description language. This is supported by HDL editor. Supported languages: Verilog and VHDL. After entering, we can check if our circuit is working properly. The control is done by simulation. The simulator of the WebPACK system is the Xilinx ISE Simulator. For simulation, the circuit must be "energized", variable signals must be given in the inputs of the circuit . This is done by test vectors. Test vectors can be specified by the designer with VHDL description (test bench). Circuits tested at the measurements were implemented by a colleague in CPLD. We had the program system in place so we chose this to test our logical networks. With the help of the simulator we examined the timing of the circuits

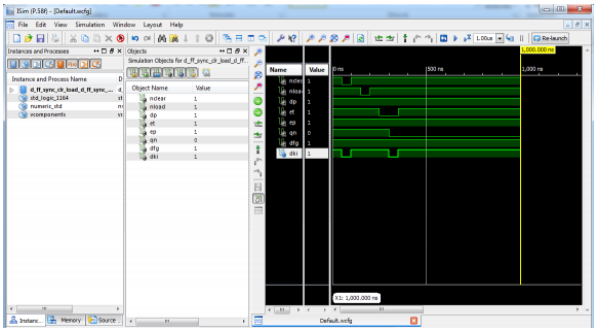


Figure 8 ISIM simulator

III. THE RESULTS OF SIMULATIONS

A. With Logisim

This program was used to test the logic of digital circuits. The circuits were built from the gates in the program library and from the basic sequential circuits (flip-flop, shift register, counters). In the case of combination networks, we have recorded the truth table with the program. It is not possible to add a status table of sequential networks because the clock cannot be considered as input by the program. For sequential circuits, we tested the outputs with the proper excitation of the inputs. We outline below the results of the simulation. When simulating a simple combination network, we have the following truth table:

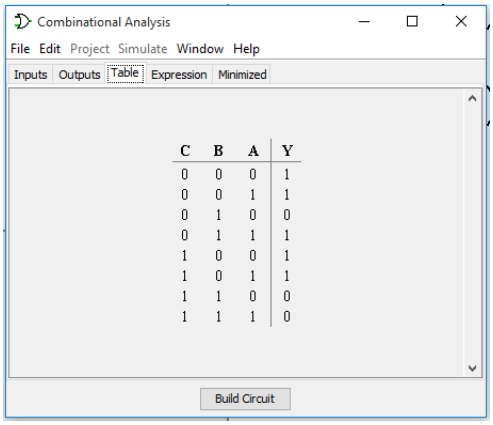


Figure 9 The truth table of simple combination circuits

In the circuit with tri-state gates, we get the following truth table

A	C	B	Y
0	0	0	x
0	0	1	1
0	1	0	0
0	1	1	!!
1	0	0	x
1	0	1	0
1	1	0	1
1	1	1	!!

Figure 10 The truth table of tri-state circuit

The output x of the output (Y) actually indicates a high impedance state when B and C are low. The „!!" means the control is prohibited when both HCT126 are enabled (B = C = 1).

At the full adder the result of the simulation is as follows:

Ci	A	B	Si	Cil
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 11 The truth table of the full adder

For sequential circuits, we could not add a state table to the program, but we tested the outputs by the excitation of the inputs. In the case of a Flip Flop Circuit, we get a sequence of states: Res-> 0,1,2 and again 0.

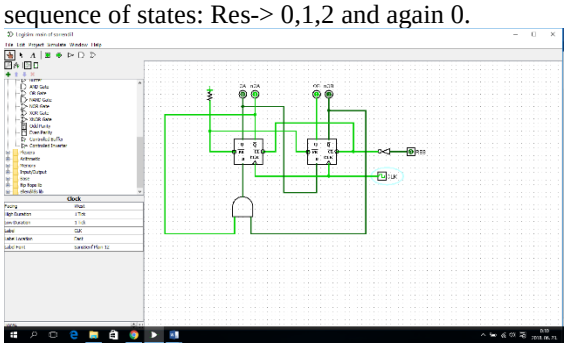


Figure 12 Simulation of the flip-flop circuit

In the case of ring counter is a sequence of states: Res-> 1,2,4,8 and again 1.

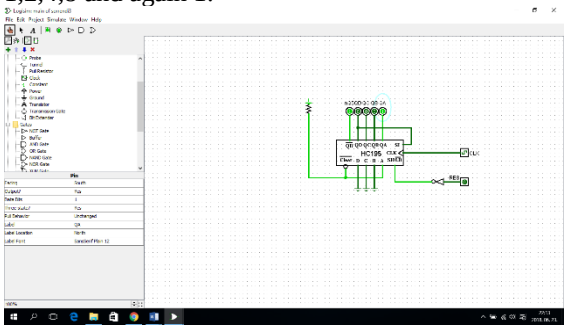


Figure 13 Simulation of the ring counter

In the case of synchronous counter is a sequence of states: Res->0,1,2,3,4,5 and again 0If the EP or ET input is 0, the circuit has not gone further, the outputs have not changed.

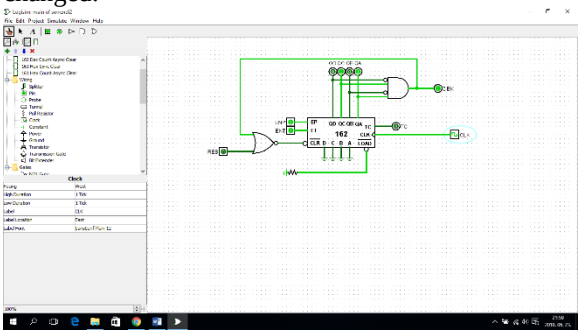


Figure 14 Simulation of the synchronous counter

We received the expected results for all the simulations.

B. With ISIM simulator [6]

In order to come closer to the properties of the circuit elements we used real components in the simulation, we have described them in VHDL as their function. Using the components in the description language of hardware (making them a symbol), we built up the combination and sequence networks outlined at the beginning of the article. Using the built-in symbols, we constructed the tested circuits with the XILINX company's free program package (ISE WebPack).

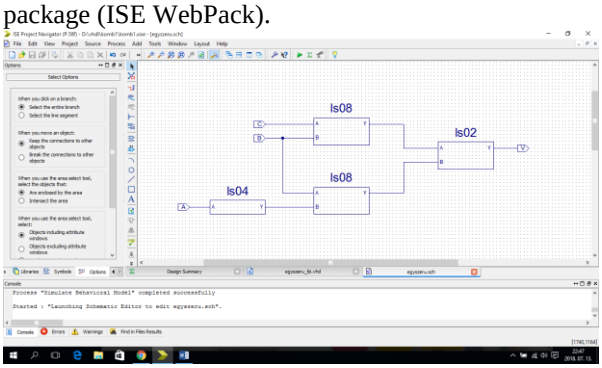


Figure 15 The implementation of a simple combination network with Ise Webpack

For the simulation of the circuits, the state of the inputs had to be determined. This was described in VHDL. After filling the test bench, we started the ISIM simulator, which outlined the circuit time diagram of the input excitation signals. The 8 possible logical values differentiated by the program are represented by different colors in the time diagram. Some colors refer to what we will need, The green color indicates a definite logic values 0 and 1. The blue color is characteristic of the high impedance state. The orange color indicates that the test signal is not determined. The red color indicates a fault simulation. The tri-state gates outputs connection, means that each tri-state gate was enabled. This control should be avoided. The clock signal period time is 100 ns for the flip-flop circuit, the clock signal period time of the shift-register and synchronous counter circuit is 200 ns. The Reset signal is high for a clock period. These were described in the test bench for each sequential circuit.

The detail of the test bench set in the ring counter is the following:

```
CLK_process :process
  begin
        CLK <= '0'; wait for CLK_period/2;
        CLK <= '1'; wait for CLK_period/2;
  end process;
-- Stimulus process
  stim_proc: process
  begin
    RES <= '0';
    wait for clk_period;
    RES <= '1';
    wait for clk_period;
    RES <= '0'; wait;
  end process;
```

In a time diagram, the delay times are also visible.

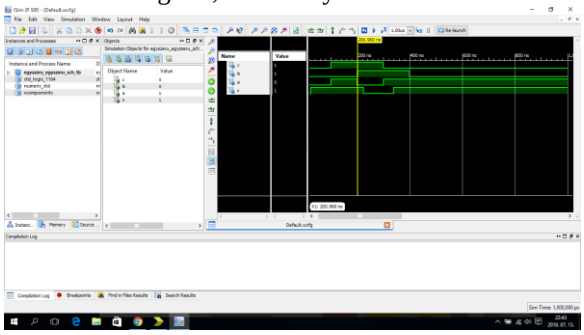


Figure 16 The simulation of simple combination network

In the simple combination network, the output is logically 0 when input B and C are 1 or B is 1 and A is 0.

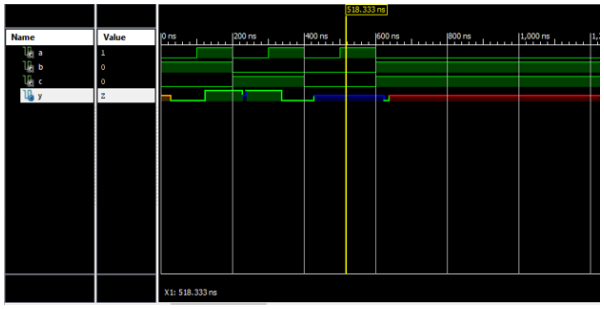


Figure 17 The time diagram of tri-state circuit

The tri-state network output is a logic value 1 when the input B is 1, the C input is 0, and A input is 1, or the C input value 1, B 0 and A is 0. The blue color indicates the high impedance state (B=C=0), the red color shows the forbidden control (B=C=1).

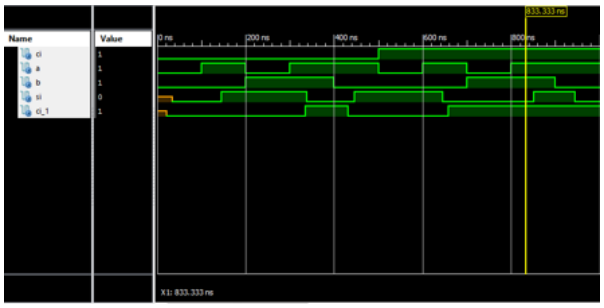


Figure 18 The time diagram of the full adder

Si output of the full adder, this is 1 if one of the A, B, Ci inputs is 1 or all 1. The Ci + 1 output is 1, if at least two inputs are 1.

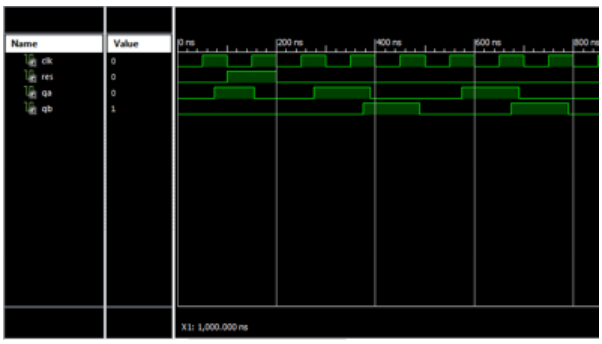


Figure 19 The time diagram of flip flop circuit

The flip-flop circuit reset to 0, then 1, 2, and again 0 will appear on the outputs.

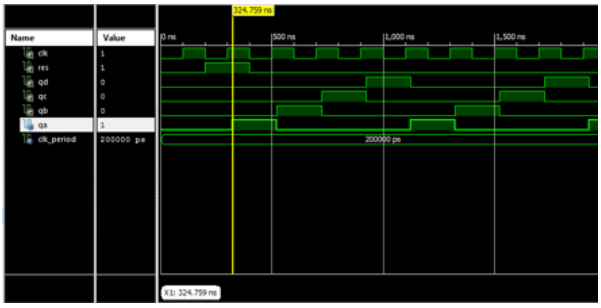


Figure 20 The time diagram of the ring counter

The ring counter to Reset 1, then 2, 4, 8 and again 1 to the outputs.

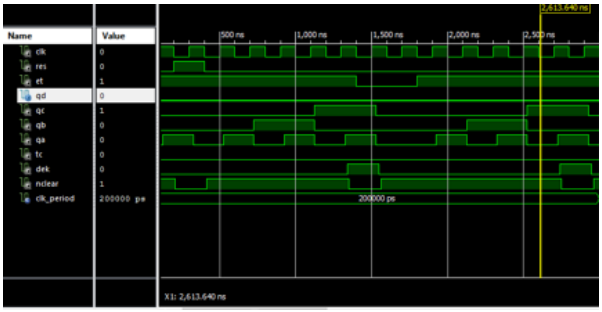


Figure 21 The time diagram of the synchronous counter

The network resets to 0, 1, 2, 3, 4, 5 and again 0. When the ET is low, the network keeps the current status.

Each simulation result was in line with expectations. In the tri-state network, due to the timing of the excitation signals, we saw spikes in the time diagram. In the case of the blue spike, tri-state gates was not allowed for very short periods of time. (Figure 22 top time diagram). Blue color indicates the high impedance state. In the case of a green spike, due to the delay times, one gate was enabled for a short time. (Figure 22 below).

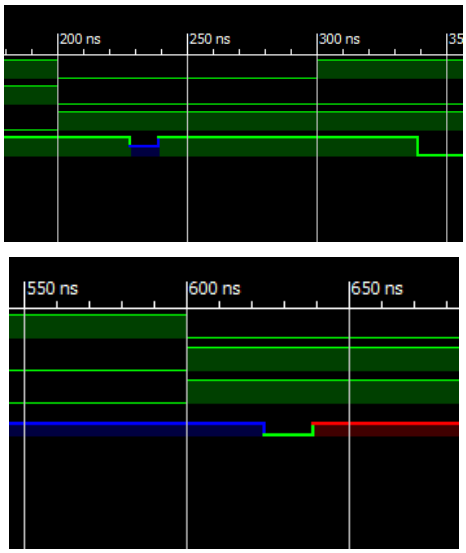


Figure 22 Tri-state network is an enlarged detail of the signals

IV. OSCILLOSCOPE MEASUREMENTS

A. The built circuit

We built the digital circuits on a test panel. We worked with on the circuit diagrams (Figures 1, 2, 3, 4, 5, 6) visible IC number. We generated input excitation signals using a microcontroller development environment. The microcontroller test environment is described in another article. [4] The built circuit operates on a 5V supply voltage. We used the T-Bird 2 AVR development platform produced by BioDigit Kft. It includes ATMEL AVR - Atmega128 microcontroller. The microcontroller panel is operated by a 5V power supply received from a USB connector of the computer or an external adapter.

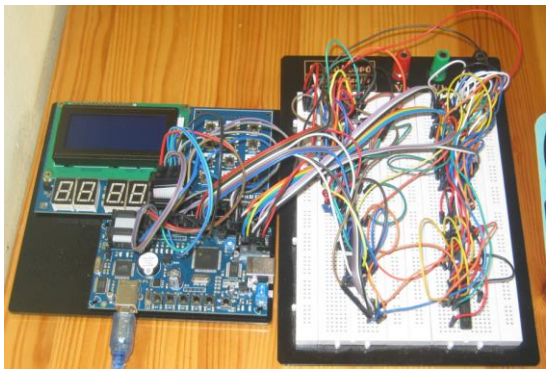


Figure 23 The circuit built on the test panel and the development environment

B. Used oscilloscope

Tektronix TDS 1012B oscilloscope was used for the measurements. is a digital storage oscilloscope with 2 channels, a separate trigger source, 100 MHz bandwidth, 1 GS / s sampling rate, and monochrome LCD display.

Figure 24 TDS 1012B oscilloscope

C. Measurement results

We generated the clock and reset signal for sequential networks by a software. The period of the clock signal is 2 ms, the reset signal is high for 1 clock cycle. We have examined the operation of all combination and sequential networks. For each measurement, the input excitation signals were generated using the microcontroller software. For oscilloscope measurements we can only examine two signals at a time, so it is a bit lengthy to examine the operation of the circuits. The triggering signal is always selected for the desired switching. The trigger came from an external source, set to edge and falling edge. For all measurements, the expected result was obtained. The following figure shows the waveforms displayed on the oscilloscope display.

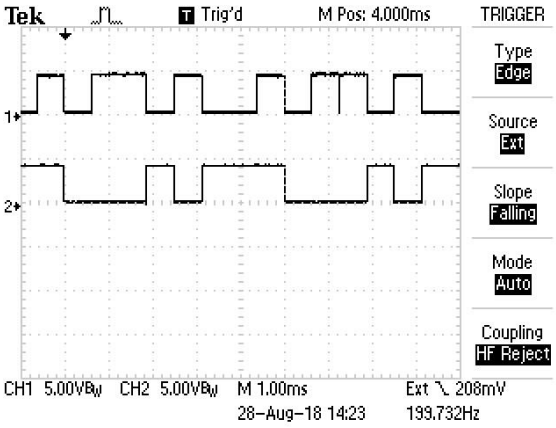


Figure 25 The waveform measured at the Si and Ci + 1 outputs of the full adder

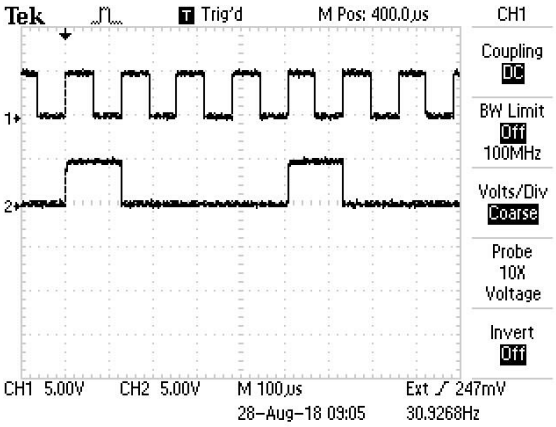


Figure 26 At the ring counter, waveforms of the clock signal and the QA output

V. COMPARISON OF VARIOUS MEASURING RESULTS

We tested three different methods for the operation of digital circuits. Out of the three methods, testing with the Logisim program is the simplest. With the help of the program we introduced the circuits and then checked their operations. We could only check the logic function with Logisim. Delay times could not be taken into account. The program gave a truth table of combination networks. For sequential networks, we manually changed the clock to check the operation of the circuits step by step. We recommend this program for beginners who are familiar with digital technology. In the second case, we tested the operation of the digital networks by the Xilinx software package with ISE WebPack. We described the operation of the circuit elements in VHDL. From the base elements we built the examined circuit, which were then examined with the ISIM simulation program. Input excitation signals are also described in VHDL. Digital networks were implemented using the schematic editor of the program package. This type of solution requires more serious knowledge. The operation of the combination and sequential networks was also examined in the form of a time table. We could measure the time data using the markers, the program is not suitable for voltage measurement. The possible logical values are indicated by different colors in the simulation program. We could not describe all the attributes of the real circuit elements in the program. There were differences between the built circuit and the simulation circuit. We could set delay times but we could not take into account setup and hold times. The period time of the clock was 100 ns and 200 ns, for the actually built circuit, this data was 2 ms. The third solution is the oscilloscopic measurement. In this case we built the circuit to be tested on the test panel. At a voltage of 5 V, we controlled our digital circuits with a microcontroller. In oscilloscope measurements, we could only examine two signals simultaneously, and the trigger signal was also important. In this case, we could accurately measure time data and measure voltage. This is lengthy, but the most accurate measurement is achieved by this method. In the built circuits, the tri-state gates (HCT126) we had to be careful not to allow both gates to be simultaneously enabled. This was not the case with the other two methods, but the built-in circuit would have caused the ICs to fail in this forbidden control.

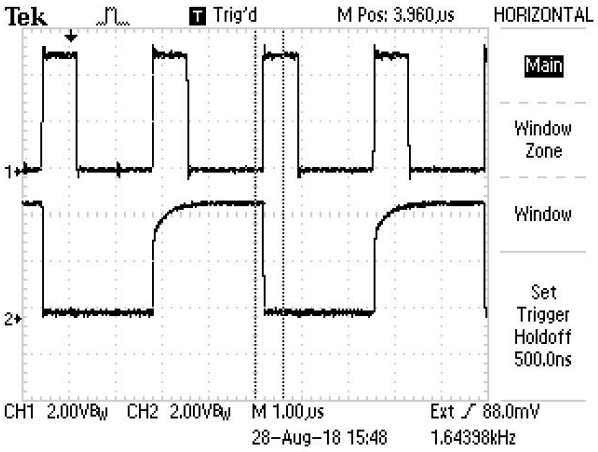


Figure 27 For a synchronous counter circuit, the clock signal and the QA output signal on the oscilloscope

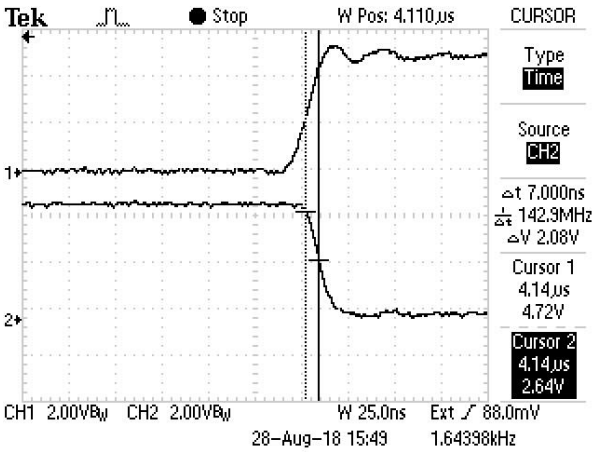


Figure 28 For synchronous counter circuit, the clock signal and QA output signal are enlarging

VI. REFERENCES

[1] http://www.cburch.com/logisim/
[2] https://www.xilinx.com/products/design-tools/ise-design-suite/ise-webpack.html
[3] https://www.xilinx.com/products/design-tools/isim.html
[4] Supervision of the Operation of Digital Circuit by Embedded Microcontroller (György Györök, András Dávid, Nikoletta Tolner, Bertalan Beszédes, Dániel Cseh)
[5] https://www.tek.com/oscilloscope/tds1012b
[6] The usage of programmable circuits in the education of Digital Technology (Nikoletta Tolner, András Dávid) AIS 2017